

IN THE CLAIMS:

Please amend claims 15 and 16, and add new claims 20-25 as follows:

15. (Amended) An integrated circuit of the type having metallization levels separated by dielectric layers and metallized vias connecting lines of different metallization levels, said integrated circuit comprising:

at least first and second metallization levels;

at least first and second superposed dielectric layers located above the first metallization level, the first dielectric layer being located on the first metallization level;

a third dielectric layer located above the first and second dielectric layers; and

at least one electrical connection element provided in the third dielectric layer and passing through the second dielectric layer until it comes into contact with the first dielectric layer.

16. (Amended) An integrated circuit of the type having metallization levels separated by dielectric layers and metallized vias connecting lines of different metallization levels, said integrated circuit comprising:

at least first and second metallization levels;

at least first and second superposed dielectric layers located above the first metallization level;

a third dielectric layer located above the first and second dielectric layers;

at least one electrical connection element provided in the third dielectric layer and passing through the second dielectric layer until it comes into contact with the first dielectric layer; and

at least one metallized via having an upper surface that is flush with an upper surface of the second dielectric layer.

Please add new claims 20-25 as follows:

--20. (New) The integrated circuit as defined in claim 15, further comprising at least one metallized via having an upper surface that is flush with an upper surface of the second dielectric layer.--

--21. (New) The integrated circuit as defined in claim 20,  
wherein the metallized via has a lateral surface adjacent to its upper surface, and  
the electrical connection element includes one portion that is in contact with the upper  
surface of the metallized via and another portion at the level of the second dielectric layer that is  
in contact with the lateral surface of the metallized via.--

--22. (New) The integrated circuit as defined in claim 18, wherein the fourth dielectric layer is  
located on the second metallization level.--

--23. (New) An integrated circuit of the type having metallization levels separated by dielectric  
layers and metallized vias connecting lines of different metallization levels, said integrated  
circuit comprising:

- at least first and second metallization levels;
- at least first and second superposed dielectric layers located above the first metallization  
level;
- a third dielectric layer located above the first and second dielectric layers;
- at least one electrical connection element provided in the third dielectric layer and passing  
through the second dielectric layer until it comes into contact with the first dielectric layer;
- a third metallization level;
- at least fourth and fifth superposed dielectric layers located above the second  
metallization level;
- a sixth dielectric layer located above the fourth and fifth dielectric layers;
- at least one additional electrical connection element provided in the sixth dielectric layer  
and passing through the fifth dielectric layer until it comes into contact with the fourth dielectric  
layer; and
- at least one additional metallized via having an upper surface that is flush with an upper  
surface of the second dielectric layer.--

- 24. (New) The integrated circuit as defined in claim 23,  
wherein the metallized via has a lateral surface adjacent to its upper surface, and  
the electrical connection element includes one portion that is in contact with the upper  
surface of the metallized via and another portion at the level of the second dielectric layer that is  
in contact with the lateral surface of the metallized via.--
- 25. (New) The integrated circuit as defined in claim 23, wherein the fourth dielectric layer is  
located on the second metallization level.--